DSP SOC Design Methodology for Digital Camera

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Digital still cameras (DSC) are rapidly proliferating as technology adds new capabilities and improves image quality and utility by allowing pictures to be printed after taking them, as well as reducing power consumption, cost, and increasing picture storage. Although numerous vendors are entering the market with products ranging from $300 to several thousands of dollars targeted at the camera-computer user and the consumer, the digital still camera is still not equivalent to the traditional film camera. This article explores the more complex design of a consumer camera, the technologies being applied today to improve DSC quality and utility, and new methodologies needed to address these complex design issues.

Today's technology consists of new types of lenses, complementary metal oxide silicon (CMOS) image sensors with analog/digital (A/D) conversion, image enhancement algorithms, improved compression, increased memory densities, improved packaging, increased integrated circuit (IC) integration, and liquid crystal display (LCD) panels or micro displays. The DSC can be a complex digital signal processing (DSP) system that delivers the best automatic image quality, which is important for a non-PC consumer, while, the simple camera with no imaging DSP is commonly tethered to a personal computer. Image processing is required because the sensor does not "see" light just like a human.

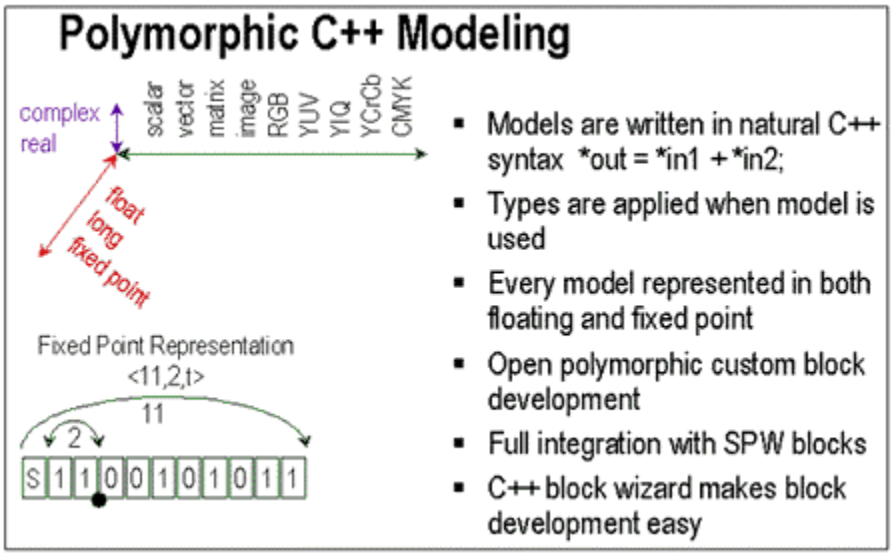
The staff requirements of a camera design methodology should include knowledge of the system components, lenses, IC design including elements of analog in the image sensor, A/D, audio, video output, image DSP, LCD interface, and interface to the PC and printer. Current design methodology incorporates various point tools to investigate and verify each stage of the design process. Typical development environments are composed of generally three distinct development teams, each of which use a variety of point tools optimized for their specific goal. The initial process in any design is algorithmic development.

This is the stage of the design process where ideas are mapped to algorithms. Typical tools used in this stage of the design process include custom C/C++ models in conjunction with popular floating-point image processing tools. Once the algorithm has been verified as functional with appropriate complexity for implementation, the next step in the design process is to determine the effects of fixed-point precision. This process typically includes re-coding the existing design using a custom fixed-point C/C++ implementation. Fixed-point implementations of image processing routines can introduce visible image quality degradation and these effects must be modeled in order to minimize them. Once the minimum bit width for acceptable image quality is established for a given algorithm, the algorithm must be implemented in register transfer logic (RTL). This process also typically includes a re-coding of the design in VHDL or Verilog hardware

description languages for a given architectural implementation. Verification at this stage of the design process often requires writing specific test cases to ensure viability of the model. Since each of the described steps in the development cycle incorporate specific modeling tools it is also difficult to verify the models with respect to each other and the ability to effectively leverage designs between the development teams is minimized. Typically, a design specification is all that can effectively be given to each group involved in the development cycle. Although this design methodology has been used successfully in the past, market pressures are forcing reduction in design cycle times.

Cadence has introduced revolutionary new polymorphic technology into its Cadence® signal processing worksystem (SPW) product extending its capabilities to overcome challenges presented in designing these systems (See Figure 1). In particular the difficulty in describing the image processing algorithms in the first place and the requirement of recapturing the algorithms to investigate fixed-point effects have nearly been eliminated. The SPW product's new polymorphic technology enables modelers to write one simple algorithmic model in C++ that is later bound to particular image types and floating or fixed-point properties. This late binding enables complex system exploration simply by changing parameters.

Figure 1



In order to accelerate each stage of the design process, the SPW product with the Cadence multimedia design kit include a base line set of imaging specific functions for rapid algorithmic development. Algorithms developed in the SPW product can automatically generate a stand alone C++ executable using the code generation system (CGS). The compiled simulation is advantageous since it has much faster run time than typical simulation engines.

As an adjunct tool, the Cadence virtual component codesign (VCC) product can be used to help determine the system architecture. Typically, IP created in SPW is exported via OMI (Open Model Interface) to VCC. VCC allows the designer to make hardware/software tradeoffs. Once a choice is made, VCC can export an integrated model

of HW/SW for coverification using Cadence's Affirma™ HW/SW verifier. Once final mapping is done, implementation of hardware can proceed.

A component of the SPW product, the Cadence hardware design system (HDS), can be used to implement these designs into architectural models for direct RTL generation. The combination of the SPW product and the multimedia design kit with HDS capability enables multiple development teams to use a single unified system development platform that effectively bridges the gaps and reduces design cycle time from the traditional methodology. Once again, the design methodology still entails all the steps mentioned previously but the different design teams can stay within a unified design environment, which can be leveraged to create the design specification. (See Figure 2)

The SPW product and HDS, along with the Affirma™ NC-Verilog simulator and the Envisia™ Ambit® synthesis tool provides an integrated flow from system specification through IC implementation and verification. The system specification is fully defined through the fixed-point level in the SPW product. The next step in the refinement path can use a mixture of HDS RTL block diagrams and hand-coded VHDL or Verilog language blocks to design the IC architecture. This mixed HDL/HDS block diagram can be verified through extremely high-performance simulation with SPW C++ models. After logic synthesis with the Envisia Ambit synthesis tool, these same mixed-level testbench/gate-level models are used for complete functional verification.

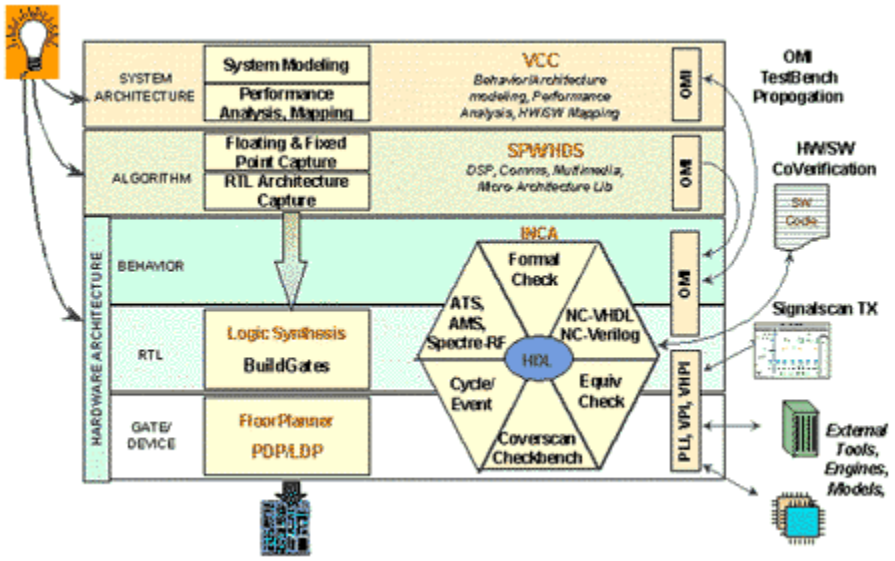
Once the model, which meets the specification, is verified, the RTL is generated directly from the verified model. These models are then completely reusable in future design enhancements across multiple teams. Another key benefit is the ability to incorporate custom pre-built C and RTL models. This environment is completely open and supports both co-simulation with HDL simulation tools and the Open Model Interface (OMI), thus providing a strong unified development environment at every stage of the design cycle.

The following describes an example of an SPW algorithm simulation applied to the first stages of the image processing. The camera image-processing path can lose image quality at many stages, for example, light is lost and noise is introduced in the lens, sensor and A/D. The algorithms that input data from the sensor should maintain the maximum useable dynamic range of the sensor while restoring the data to normalized color and intensity for the compression and viewfinder stages. Auto-focus, white-balance, and color interpolation, sometimes called demosaic, are algorithms that optimize image quality. Following color interpolation and other algorithms, the compression stage may also lose some image quality in trade for a reduced storage requirement in Flash or Disk memory.

Color interpolation is a key algorithm to maximizing image quality. The image sensor chip detects the intensity of light after it passes through a color filter. A common method to capture a color image is to integrate the color filters onto the image sensor itself, selecting a single filter color for each pixel site in such a way that the full-color image can be reconstructed from this "color mosaic" image. This color mosaic filter, or color filter array is usually a thin layer of color dyes that is the top layer of the image sensor semiconductor. The color filter array (CFA) allows the sensor to measure only a single color component at each location, thus a processing step is required to convert the CFA image into a full-color image, with all three-color components at each location. That step

is called *color interpolation*, because it must interpolate or predict the sampled color values to estimate the missing color components at each site. This estimating step, which uses power and affects shots-per-second, is critical in obtaining a quality image from a CFA image sensor.

Figure 2



Power constraints in battery-powered devices cause a severe limit on the amount of processing that can be done in a digital camera. The cost constraints on the camera also limit the available processing power. Due to these constraints, the color interpolation step must be reasonably efficient if it is to go inside the camera. In digital cameras, achieving acceptable battery life, cost, and shots-per-second are already significant challenges, so low algorithm complexity is of critical importance.

A common color filter array pattern for digital cameras is the Bayer 2G pattern, which contains two green filters for each red and blue filter. There are more green sensors than red or blue because the human eye is more sensitive to green. For this sensor one of the simplest interpolation methods is known as linear interpolation. In this method, to estimate a missing color at a particular site, the neighboring known pixels of the same color are examined, and a linear combination (3 by 3) of them is used to create the missing color. This method has the advantage of being fast and simple, but the resulting image quality is poor. Typical problems with this method are "zipper" artifacts, false colors along edges, and an overall loss of image sharpness.

During the design process, image quality is paramount and artifacts or improvements should be observable. The Multimedia design kit can help establish and manage image quality of the DSP algorithms both subjectively and numerically. The Multimedia design kit enables verification across reference images, comparison of algorithms, and optimization of fixed-point effects. At any point in the system, model information or images can be examined as a picture or numerically analyzed and displayed. To complement the modeling environment, the multimedia design kit also provides interactive visualization tools called the video viewer and the image quality tester. The video viewer utility presents the resulting images from a model simulation in real-time

for subjective analysis of artifacts. The image quality tester provides state-of-the-art image analysis functions that closely mimic human perception of image quality. Thus, in an automated process, the simulation can proceed through different input images, algorithms, and fixed-point evaluations.

To further accelerate the design of the camera, Cadence offers a service that provides the behavioral model of the selected CMOS or charge coupled device (CCD) sensor. This model reflects the specification of a sensor that is in design by a silicon vendor but will not be available until the camera prototype is near complete. This is a more common situation as new design methodology reduces time-to-market. Cadence also provides design methodology services. A designer may evaluate several virtual sensors (mixed-signal) with combinations of DSP algorithms to determine the optimal system design.

Iterated Systems Inc. (www.iterated.com) evaluated its new color interpolation algorithm in a camera model, within the SPW product and quickly determined that their method was superior to linear interpolation that is used in some cameras today. The images resulting from this new method have fewer artifacts and sharper details, producing the best quality images from any CFA image sensor they tested in the SPW product.

The Cadence system-on-a-chip (SOC) DSP design flow has improved productivity via polymorphic algorithm capture, significant library content and tools for managing image quality during the design and verification process. Cadence will continue to improve this design methodology to help customers bring digital imaging products to market faster.