High Efficiency Eight Output, 60 W Set Top Box Power Supply Design

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APPLICATION NOTE

INTRODUCTION/ABSTRACT

Due to their use in high volume consumer applications where minimum cost is the driving factor, set−top box power supplies have typically been minimally designed and usually result in low performance, low efficiency power sources. The compromises in such designs can also result in poor reliability and hot internal operation of the set−top box circuitry. The reference design presented in this application note demonstrates that a multi−output STB power supply can be designed with efficiencies approaching 80% utilizing low cost ON Semiconductor power management ICs and semiconductors along with the standard passive components required. The key to the design is the use of a quasi−resonant, critical conduction mode flyback topology utilizing the NCP1207A controller, the use of the NCP1582 high efficiency synchronous buck regulator controller to derive the supply's lowest output voltages, and an optimal flyback transformer design.

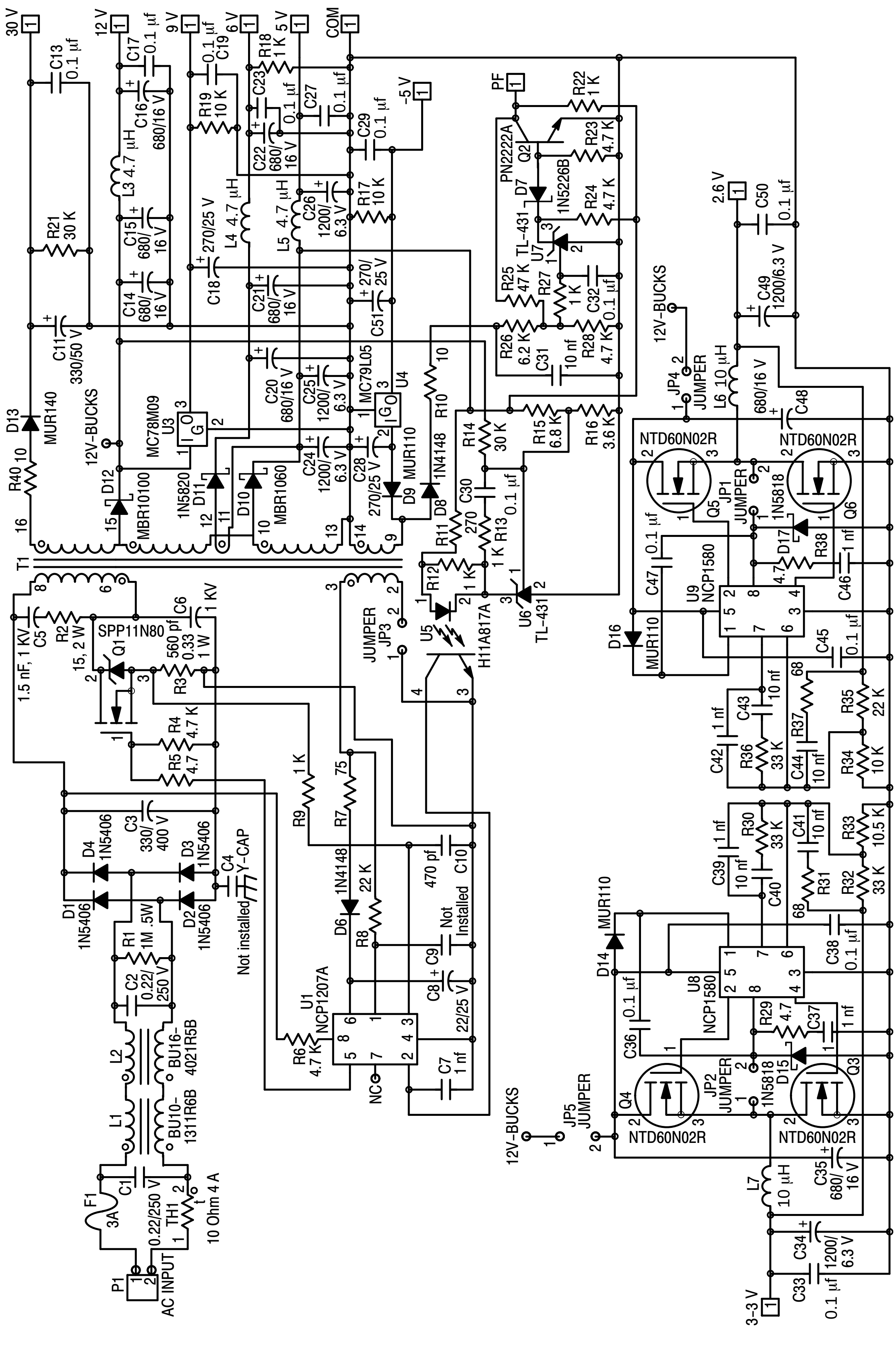
Most STB power supplies provide from three to eight regulated and/or quasi−regulated outputs with typical power levels from 30 to 90 W. This particular reference design provides eight outputs at a continuous output power of 60 W and an output surge rating to 90 W with a universal input voltage of 90 to 265 Vac. The design is constructed around a single−sided, open−frame printed circuit board with the dimensions of 9.5″L x 3.15″W x 1.9″H. There is sufficient latitude in the selection of components that other variations of this footprint and overall design can be realized. In order to keep cost minimized, the AC input is of the two−wire type and a simple two stage, common mode EMI filter is utilized for conducted EMI compliance. The outputs are interfaced with the load via flying wire leads. Heatsinking on critical semiconductors is accomplished with inexpensive, stamped sheet metal heatsinks which solder mount vertically onto the pc board. For low output ripple and noise, pi−network filters are implemented using off−the−shelf slug core inductors and low ESR electrolytic capacitors.

General Specifications

Input: 90 to 265 Vac, 47–63 Hz
Inrush Current: 30 A cold start; 60 A warm start
Efficiency: 75% or better at nominal loading for universal input (measured at 115 and 230 Vac)
Output Voltages/Regulation/Ripple:

Channel	Vout	Output Type	Regulation	Max Ripple	Current	Surge
1	2.6 V	Buck Reg.	±1%	40 mVp/p	3.0 A	4.0 A
2	3.3 V	Buck Reg.	±1%	40 mVp/p	4.0 A	5.0 A
3	5.0 V	Main Output	±2%	50 mVp/p	3.0 A	4.0 A
4	6.2 V	Quasi−Reg.	±6%	50 mVp/p	1.5 A	2.0 A
5	9.0 V	3−T Reg.	±1%	30 mVp/p	100 mA	200 mA
6	12 V	Main Output	±2%	50 mVp/p	1.0 A	3.0 A
7	30 V	Quasi−Reg.	±8%	100 mVp/p	20 mA	40 mA
8	−5.0 V	3−T Reg.	±1%	30 mVp/p	30 mA	60 mA

Output Overshoot: 5% max; typically <1%
Overcurrent/Short Circuit Protection: Protected against accidental overloads via reduced duty cycle, burst mode operation
No Load: Output voltages are controlled and stable under no load conditions
Temperature: Operation from 0 to 50°C (no overtemp protection included in reference design)


30 V
12 V
9 V
6 V
5 V
COM
-5 V
PF
2.6 V
3-3 V
AC INPUT
P1
F1
3A
TH1
10 Ohm 4 A
C1
0.22/250 V
L1
L2
BU10-1311R6B
BU16-4021R5B
C2
0.22/250 V
R1
1M .5W
D1
1N5406
D2
1N5406
D3
1N5406
D4
1N5406
C3
330/400 V
C4
Y-CAP
Not installed
U1
NCP1207A
NC
C7
1 nf
C8
22/25 V
C9
Not Installed
C10
470 pf
R6
4.7 K
R7
75
R8
22 K
R9
1 K
D6
1N4148
Q1
SPP11N80
R2
15, 2 W
C5
1.5 nF, 1 KV
C6
560 pf
1 KV
R3
0.33
1 W
R4
4.7 K
R5
4.7
T1
U5
H11A817A
JP3
JUMPER
U6
TL-431
D13
MUR140
R40
10
C11
330/50 V
C13
0.1 µf
R21
30 K
D12
MBR10100
12V-BUCKS
U3
MC78M09
D11
1N5820
D10
MBR1060
L3 4.7 µH
L4 4.7 µH
L5 4.7 µH
C14
680/16 V
C15
680/16 V
C16
680/16 V
C17
0.1 µf
C18
270/25 V
C19
0.1 µf
R19
10 K
C20
680/16 V
C21
680/16 V
C22
680/16 V
C23
0.1 µf
R18
1 K
C24
1200/6.3 V
C25
1200/6.3 V
C26
1200/6.3 V
C27
0.1 µf
C28
270/25 V
C29
0.1 µf
C51
270/25 V
U4
MC79L05
R17
10 K
D9
MUR110
D8
1N4148
R10
R11
270
R12
1 K
R13
1 K
C30
0.1 µf
R14
30 K
R15
6.8 K
R16
3.6 K
Q2
PN2222A
R22
1 K
R23
4.7 K
D7
1N5226B
R24
4.7 K
U7
TL-431
R25
47 K
R26
6.2 K
R27
1 K
R28
4.7 K
C31
10 nf
C32
0.1 µf
JP4
JUMPER
L6 10 µH
C48
680/16 V
C49
1200/6.3 V
C50
0.1 µf
Q5
NTD60N02R
Q6
NTD60N02R
JP1
JUMPER
D17
1N5818
R38
4.7
C46
1 nf
U9
NCP1580
C47
0.1 µf
D16
MUR110
C45
0.1 µf
C42
1 nf
C43
10 nf
R36
33 K
C44
10 nf
R37
68
R35
22 K
R34
10 K
C39
1 nf
C40
10 nf
R30
33 K
C41
10 nf
R31
68
R32
33 K
R33
10.5 K
D14
MUR110
U8
NCP1580
C36
0.1 µf
C38
0.1 µf
R29
4.7
C37
1 nf
Q4
NTD60N02R
Q3
NTD60N02R
JP2
JUMPER
D15
1N5818
JP5
JUMPER
L7
10 µH
C35
680/16 V
C34
1200/6.3 V
C33
0.1 µf

Circuit Design and Operation

Referring to the schematic in Figure 1, the AC input is fused via F1 and inrush current limiting is provided by TH1, a negative temperature coefficient thermistor. C1, L1 and L2, C2 comprise a two stage common and differential mode EMI filter. Differential mode filtering is accomplished via the leakage inductance of the two inductors. Full−wave rectification of the line voltage is accomplished by D1 through D4 producing a nominal bulk voltage of 165 to 320 Vdc on C3.

The basic converter stage is comprised of duty cycle controller U1, MOSFET switch Q1, and flyback transformer T1 and its associated secondaries and secondary rectifiers. The flyback converter operates in critical conduction mode in which the energy stored in the flyback transformer T1 is allowed to just go to zero before Q1 can switch on again. The NCP1207A is a current mode duty cycle controller which monitors the MOSFET peak current via R3. The peak current level is set by the feedback loop voltage which is coupled to the controller through optocoupler U5 for safety isolation. U6, a TL431 programmable Zener, is utilized as the output voltage sense amplifier. Both the 5.0 V and 12 V outputs are sensed via the summing junction created by R14, 15 and 16. This summing technique enhances the load regulation on both outputs with little degradation of cross regulation effects between the two outputs.

The status of the flyback or reset voltage on T1 is monitored by the lower auxiliary winding on the transformer through R8. This prevents the MOSFET from turning on before the flyback energy is completely depleted from the transformer. As a consequence, the basic operation of the converter results in a combination of variable frequency, variable pulse width control of the transformer primary winding. This technique has significant advantages over fixed frequency flyback operation in that the MOSFET current always starts at zero, and, because of the circuitry in the NCP1207 chip, the turn−on of the MOSFET can be made to occur at the valley or low point of the flyback ringout voltage, resulting in a quasi−resonant circuit operation with decreased Miller Effect losses in the MOSFET. The flyback valley detection for turn−on is further enhanced with respect to noise immunity by adding a small amount of additional capacitance across the MOSFET and/or the flyback transformer primary with C5 and C6. C5 includes series damping resistor R2 which reduces the voltage ringing at MOSFET turn−off caused by the leakage inductance of T1 and the resonant capacitors. Additional technical information and theory about quasi−resonant, critical conduction mode flyback switching can be obtained in the ON Semiconductor application notes mentioned in the references at the end of this document.

The auxiliary zero−current detection winding on the transformer also provides a “bootstrap” V_{CC} for U1 via R7 and D6 once the power supply starts. This reduces dissipation and de−activates the DSS (dynamic self supply) circuit in U1 during normal operation. If one of the power supply outputs is overloaded to the extent that the peak inverter current produces greater than 1.0 V across sense resistor R3, the duty cycle of the NCP1207 will be reduced. If R7 is selected such that the auxiliary winding voltage on C8 drops below approximately 10 V during the overload condition, then U1 will shut down and attempt to re−start after a time delay due to activation of the DSS circuit and the overcurrent condition presented at the current sense pin. This will result in a drastically reduced duty cycle operation of the converter with reduced output voltage and current. This “hick−up” or burst mode operation will continue until the overcurrent condition is removed. The details of the internal chip operation during this mode and normal operating modes can be found in ON Semiconductor’s NCP1207A device data sheet.

Voltage feedback is accomplished using the conventional TL431 programmable Zener (U6) and an optocoupler (U5) to drive the NCP1207A’s feedback pin. Voltage sensing is done on both the 12 V and 5.0 V outputs and summed via resistors R14, 15, and 16. This provides improved overall cross regulation for these and the 30 V output.

The 2.6 V and 3.3 V outputs are derived from the 12 V output using NCP1582 synchronous buck controllers (U8 and U9). The switching frequency is fixed at 350 kHz allowing for small output inductors and capacitors along with good transient response. ON Semiconductor NTD60N02 low voltage MOSFETS are used as the synchronous rectifier switches in both of the buck converters. The NCP1582 also monitors the on−state resistance of the upper MOSFET and will shut the drive down to the MOSFETS if the voltage drop exceeds a certain level when the device is on. This scheme provides additional overcurrent protection in the event of a shorted or overloaded buck converter output.

A simple, but very effective AC power fail detection circuit is implemented utilizing another TL431 as a level comparator (U7) which senses the reflected peak of the inverter bulk voltage via the −5.0 V output winding on T1 through forward sensing diode D8. The power fail output is from the collector of Q2 and hysteresis is provided by R25 to avoid jitter at the PF transition point. This circuit will provides approximately 5.0 ms minimum of warning time before any of the power supply outputs drop to 90% of nominal value.

Magnetics Design

The key to designing a simple, low cost yet effective regulated multiple output power supply such as this lies in the magnetics design. The flyback transformer must have low leakage inductance to minimize cross−regulation effects and unwanted voltage spikes. The secondary turns and output diode configuration must also be designed so that the necessary output voltages can be achieved without the proliferation of separate regulator circuits for every output. For proper output voltage set points the secondary turns must be chosen correctly since integral numbers of turns must be used. For this design the +5.0 V, 6.0 V, 12 V and 30 V outputs are all derived from a “stacked” winding configuration. The 9.0 V output is derived from the 12 V output using a three−terminal linear regulator only because the specified maximum output current was so low. Likewise with the −5.0 V output, a three−terminal regulator was used with a separate transformer winding because of the low current requirement.

Referring to the magnetics design information of Figure 2, the secondary turns for the 5.0 V and 12 V windings were configured using seven turns of copper foil. Foil was necessary to minimize leakage inductance because of the small number of turns involved. The full seven turns developed the 12 V output while a tap at the 4^{th} turn (from the 12 V “high” side) provided the 5.0 V output. For the 6.25 V output a separate, single turn of foil was necessary because, in order to keep this output voltage from being excessive, one side of the winding had to be connected to 5.0 V rectifier diode D10’s *cathode* (see Figure 1 schematic.) Note that this subtracts an additional 0.45 V diode drop from the voltage developed from this single turn thus preventing the output from being in the range of 6.7 V. The 30 V output is developed by a conventional single layer ten turn wire winding that is “stacked” onto the top of the 12 V winding. The total secondary winding configuration allows for very good voltage set point and cross−regulation for the +5.0, 6.0, 12, and 30 V windings. It should be noted that the 3.3 V output could have been easily derived off of the 2nd turn of the seven turn foil winding if some overall efficiency could have been sacrificed.

Project: 65 watt set−top box

Part Description: Flyback transformer, 50 kHz (QR), 65 watt, universal input

Schematic ID: T1

Core Type: ETD−39, 3C90 or P material

Core Gap: Gap for 310 uH nominal on primary

Inductance: 300 − 320 uH on primary

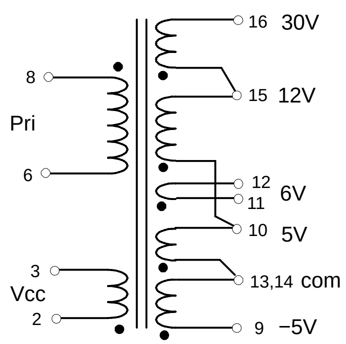
Bobbin Type: 16 pin horizontal pc mount (Ferroxcube PC1−38H or equivalent)

Windings (in order):

Winding # / type	Turns / Material / Insulation Data
Vcc/Demag (2 − 3)	6 turns of #24HN spiral wound over bobbin with 0.20” end margins. Self−leads to pins. Insulate with 2 layers of tape.
Primary (8 − 6)	42 turns of #24HN over 1 layer with tape cuffed ends. Self−leads to pins. Insulate for 3 kV to next winding with tape.
5V/12V stacked sec. (13, 14 − 10 − 15)	7 turns of 5 mil thick foil x 0.75” wide in center of bobbin. Tap at turn 3 with #20 wire (5V tap) and terminate start end and finish end with #20 wire. Wire can be insulated or sleeved. Connect to bobbin pins as shown below.
6V turn (11 − 112)	1 turn of 5 mil thick foil x 0.75” wide over previous secondary. Terminate with insulated #20 wire and wire to pins. Insulate with a couple layers of mylar tape.
30V secondary (15 − 16	10 turns of #24 HN spiral wound over 6V secondary. Self−leads to pins. Insulate with a couple of layers of tape.
−5V secondary (9 − 13	4 turns of #24HN spiral wound over 30V secondary. Self−leads to pins and final insulation on top. VACUUM VARNISH

Hipot: 3 kV from primary/Vcc to all other secondary windings.

Schematic



Lead Breakout / Pinout

(bottom view)

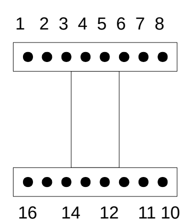


Figure 1. Magnetics Design Data Sheet

Performance Results

The test results for the power supply are tabulated in the spreadsheet of Figure 3. It should be noted that 5% resistors were used to calibrate the set−points of the regulated output voltages. The use of 1% resistors could have tightened the set−points closer to the nominally specified values. Typical efficiencies were in the mid to upper 70% range at the specified nominal loads. The efficiency is significantly affected by the loading profile and is slightly less at 230 Vac input. For 90 to 135 Vac input only applications, the output rectifiers for the 5.0 V and 12 V outputs can be replaced with lower voltage rated Schottky diodes for a 2 to 3% improvement in efficiency. Depending on the specific output voltage requirements for the set−top box application, one may also be able to eliminate the linear regulators to further improve efficiency.

Table 1. Test Data for Set Top Box Power Supply

Regulation Data (115 Vac Input)				Outputs					
Parameter	2.6 V	3.3 V	5.0 V	6.0 V	9.0 V	12 V	30 V	Neg 5.0 V	
Output Type	Buck	Buck	Main	Quasi−reg	3−T reg	Main	Quasi−reg	3−T reg	
Vout Setpoint at Typical Loads	2.53 V	3.4 V	4.89 V	6.27 V	8.94 V	12.54 V	31.0 V	4.96 V	
Vout Setpoint at Minimum Loads	2.55	3.42	4.96	6.38	8.94	12.33	32.7	4.98	
Vout Setpoint at Maximum Loads	2.54	3.34	4.9	6.29	8.94	12.53	30.1	4.95	
Vout Setpoint at No Output Loading	2.56	3.43	5.02	6.54	8.93	12.13	29.6	4.97	

Note: Vout setpoints measured at PC board
Line Regulation with input increased to 230 Vac: Less than 30 mV delta on any output

Output Ripple (@ Max loads)	27 mV	45 mV	50 mV	50 mV	40 mV	30 mV	100 mV	20 mV	(10:1 scope probe)
Output Overshoot (Turn−on)	none	none	none	none	none	none	none	none	
Efficiency Measurements									
Output Voltage	2.54	3.42	4.91	6.31	8.94	12.48	30.06	4.96	
Output Current	3.8 A	2.9 A	1.56 A	1.3 A	91 mA	1.0 A	30 mA	73 mA	
Output Power (W)	9.65	9.92	7.66	8.2	0.81	12.48	0.9	0.36	(49.98 W total)

Total Pout = 50 W
Pin at 115 Vac = 64 W => Efficiency = 78%
Pin at 230 Vac = 66.7 W => Efficiency = 75%

Table 2. Universal Input Set−Top Box BOM

Description/Part Type	Quantity	ID	Footprint/Package	Vendor	Comments
SEMICONDUCTORS					
1N5406 Diode	4	D1, 2, 3, 4	Axial, DO−201	ON Semiconductor	
MUR140	1	D13		ON Semiconductor	
MUR110	3	D9, 14, 16		ON Semiconductor	
1N4148 or 1N914A	2	D6, D8		ON Semiconductor	
1N5818	2	D15, D17		ON Semiconductor	
1N5820	1	D11	DO−201	ON Semiconductor	Cathode soldered to heatsink
MBR1060	1	D10	TO−220 on HS	ON Semiconductor	
MBR10100	1	D12	TO−220 on HS	ON Semiconductor	
NTD60N02R MOSFET	4	Q3, 4, 5, 6	DPAK, Long Lead	ON Semiconductor	
SPP11N80C3	1	Q1	TO−220 on HS	Infineon	Infineon “Cool MOS”
Optocoupler − H11A817A	1	U5	4 Pin TH	Vishay	
TL−431	2	U6, U7	TO−92	ON Semiconductor	
NCP1207A	1	U1	PDIP−8	ON Semiconductor	
NCP1582	2	U8, U9	SOIC−8	ON Semiconductor	
2N2222A NPN Xstr	1	Q2	TO−92	ON Semiconductor	
1N5226B, 3.3 V Zener	1	D7	Axial Lead	TBD	
MC78M09 9.0 V Regulator	1	U3	TO−220	ON Semiconductor	
MC79L05 −5.0 V Regulator	1	U4	TO−92	ON Semiconductor	
CAPACITORS					
330 μF, 400 Vdc Electrolytic	1	C3	LS = 0.4″, D = 25 mm	UCC	“Snap−in” Type
22 μf, 50 V Elect.	1	C8	LS = 0.1″	UCC	FL 25 VB 222 M 6x5 LL
1200 μf, 6.3 V	5	C24, 25, 26, 34, 49	LS = 0.15″, D = 10 mm	UCC	FL 6.3 VB 122 M 8x20 LL
680 μf, 16 V	9	C14, 15, 16, 20, 21, 22, 28, 35, 48	LS = 0.15″, D = 8.0 mm	UCC	FL 16 VB 681 M 8x20 LL
270 μf, 25 V	2	C18, 51	LS = 0.15″, D = 8.0 mm	UCC	FL 25 VB 271 M 8x12 LL
330 μf, 50 V	1	C11 (C12 Omitted)	LS = 0.15″, D = 10 mm	UCC	KME 50 VB 331 M 10x20 LL
560 pf, 1.0 kV Ceramic	1	C6	Disc, LS = 0.25″	Vishay	2DF0T56
1.5 nF, 1.0 kV Ceramic	1	C5	Disc, LS = 0.25″	Vishay	
0.22 to 0.47 μf, “X” Caps	2	C1, C2	LS = 22.5 mm	TBD	
470 pf, 50 V Monolythic	1	C10	LS = 0.15″	TBD	
1.0 nf, 50 V Monolythic	5	C7, 37, 39, 42, 46	LS = 0.15″	Vishay	k 102 K 15 COG F 5 T L 2
0.1 μf, 50 V Mono.	14	C13, 17, 19, 23, 27, 29, 32, 30, 33, 36, 38, 45, 47, 50	LS = 0.2″	Vishay	HY950
10 nf, 50 V Mono.	5	C31, 40, 41, 43, 44	LS = 0.15″	Vishay	k 103 K 15 COG F 5 T L 2

Table 2. Universal Input Set−Top Box BOM (continued)

Description/Part Type	Quantity	ID	Footprint/Package	Vendor	Comments
RESISTORS					
1.0 M, 0.5 W, Metal Film	1	R1	Axial Lead		
0.33 Ω, 1.0 W, Non−inductive	1	R3	Axial Lead		
15 Ω, 2.0 W, Metal Film	1	R2	Axial Lead		
4.7 Ω, 1/4 W Metal Film	3	R5, 29, 38	Axial Lead		
10 Ω, 1/4 W, mf	2	R10, R40	Axial Lead		
68 Ω, 1/4 W	2	R31, R37	Axial Lead		
75 Ω, 1/4 W	1	R7	Axial Lead		Forces skip mode in overcurrent
270 Ω, 1/4 W	1	R11	Axial Lead		
1.0 K, 1/4 W	6	R9, 12, 13, 18, 22, 27	Axial Lead		R9 sets skip mode level
3.6 K, 1/4 W	1	R16	Axial Lead		R16 sets 5.0 Vout/12Vout level
4.7 K, 1/4 W	5	R4, 6, 23, 24, 28	Axial Lead		
6.2 K	1	R26	Axial Lead		Power Good set point
6.8 K, 1/4 W	1	R15	Axial Lead		
10 K, 1/4 W	3	R17, 19, 34	Axial Lead		R34 sets 2.5 Vout level
10.5 K, 1/4 W	1	R33	Axial Lead		Sets 3.3 Vout level
22 K, 1/4 W	2	R8, R35	Axial Lead		
30 K, 1/4 W	2	R14, R21	Axial Lead		
33 K, 1/4 W	3	R30, 32, 36	Axial Lead		
47 K, 1/4 W	1	R25	Axial Lead		
Thermistor, 10 Ω, 4.0 A	1	TH1	LS = 0.3 (?)	TBD	
Fuse Clips, 3.0 A Fuse		F1			
AC Input Connector	1	Customer Supplied		TBD	
MAGNETICS					
Output Ripple Chokes	2	L3, 4, 5	D = 0.5″, LS = 0.42″	Coilcraft	PCV−0−472−03
			Wire D = 0.035″		
EMI Inductor	1	L1		Coilcraft	BU10−1311R6B
EMI Inductor	1	L2	L2	Coilcraft	BU16−4021R5B
Buck Chokes, 10 μH, 5.0 A	2	L6, L7	D = 0.5″, LS = 0.42″	Coilcraft	PCV−0−103−05
			Wire D = 0.042″		
Flyback Transformer (ETD39)	1	T1	ETD39 with 16 pins	Mesa Pwr	See Drawing
Heatsink	4	For Q1, D10, D11, D12	For TO−220, Vertical	l	Thermalloy #542502d00000
PCB, 0.063″, Single Sided	1				

References

Please see ON Semiconductor’s website (www.onsemi.com) for the following relevant application notes and the NCP1207A and NCP1580 data sheets:

AND8145/D: A 75 W TV Power Supply Operating in Quasi−Square Wave Resonant Mode Using NCP1207 Controller

AND8112/D: A Quasi−Resonant SPICE Model Eases Feedback Loop Designs

AND8129/D: A 30 W Power Supply Operating in A Quasi−Square Wave Resonant Mode

AND8127/D: Implementing NCP1207 in QR 24 W AC/DC Converter with Synchronous Rectifier

AND8089/D: Determining the Free−Running Frequency for QR Systems

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